

**In the Claims**

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently amended) A ROM circuit including memory cell columns, each column being connected to a bit line, wherein the columns are arranged in groups of two adjacent columns, each column in a group being selectable ~~selectively activable or inactivable~~ with respect to the other column in the group ~~[[of]]~~ by an activation line, wherein each column in a group is connected by one end to ~~[[the]]~~ another activation line that selects ~~[[of]]~~ the other column in the group.
2. (Previously presented) The memory circuit of claim 1, wherein the activation line of a column is brought to a ground potential to deactivate said column.
3. (Previously presented) The memory circuit of claim 1, wherein a column comprises a plurality of memory cells in series, each memory cell comprising a MOS transistor, a drain, respectively a source, of which is coupled either to a source, respectively a drain, of an adjacent memory cell, or to an end of the column.
4. (Previously presented) The memory circuit of claim 3, wherein each column of a group comprises a selection means capable of selectively activating/deactivating said column, controlled by the activation line of the column.
5. (Previously presented) The memory circuit of claim 4, wherein the selection means of a column comprises a MOS transistor in series with the memory cells of the column and arranged at the end of the column not connected to the activation line of the other column of the group.
6. (Previously presented) The memory circuit of claim 1, including an amplifier connected to the bit lines connected to the two columns of a same group.

7. (Previously presented) The memory circuit of claim 6, wherein the amplifier includes a means for invalidating the information present on the bit line connected to the deactivated column in the group.

8. (Previously presented) The memory circuit of claim 6, wherein the amplifier includes a means for lowering the voltage present on the bit line connected to the deactivated column in the group.

9. (New) A memory circuit, comprising:  
a first column of memory cells coupled to a first bit line;  
a second column of memory cells coupled to a second bit line;  
a first block select line that provides a first signal to select the first column, the first block select line being coupled to the first column and the second column; and  
a second block select line that provides a second signal that is complementary to the first signal, the second block select line being coupled to the first column and the second column.

10. (New) The memory circuit of claim 9, wherein the first block select line is coupled to a gate of a first column selection transistor, the first column selection transistor being in the first column of memory cells.

11. (New) The memory circuit of claim 10, wherein the first column selection transistor is in series with the first column of memory cells.

12. (New) The memory circuit of claim 9, wherein the first block select line is coupled to an end memory cell in the second column of memory cells.

13. (New) The memory circuit of claim 12, wherein the end memory cell comprises a MOS transistor and the first block select line is coupled to a source and/or drain of the MOS transistor.

14. (New) The memory circuit of claim 9, wherein the second block select line is coupled to a gate of a second column selection transistor, the second column selection transistor being in the second column of memory cells.

15. (New) The memory circuit of claim 9, wherein the second block select line is coupled to an end memory cell in the first column of memory cells.

16. (New) The memory circuit of claim 9, wherein the first block select line is coupled to an end memory cell in the second column of memory cells, and wherein the second block select line is coupled to an end memory cell in the first column of memory cells, the end memory cell in the second column of memory cells and the end memory cell in the first column of memory cells being on opposite column ends.

17. (New) The memory circuit of claim 9, wherein the first bit line and the second bit line are both coupled to an amplifier.

18. (New) The memory circuit of claim 17, wherein the first block select line and the second block select line are both coupled to respective inputs of a single differential amplifier.

19. (New) The memory circuit of claim 9, wherein the first column of memory cells is adjacent to the second column of memory cells.

20. (New) The memory circuit of claim 9, wherein the first block select line provides a ground voltage to the second column of memory cells when the second column of memory cells is selected.

21. (New) The memory circuit of claim 9, wherein the second block select line provides a ground voltage to the first column of memory cells when the first column of memory cells is selected.

22. (New) The memory circuit of claim 9, wherein odd columns of memory cells in the memory circuit are selected by the first block select line, and wherein even columns of memory cells in the memory circuit are selected by the second block select line.

23. (New) The memory circuit of claim 9, wherein the first block select line provides a logic 1 signal to select the first column of memory cells.

24. (New) The memory circuit of claim 9, wherein the first block select line provides a logic 1 signal when the second block select line provides a logic 0 signal.

25. (New) The memory circuit of claim 9, wherein the first block select line provides a logic 0 signal when the second block select line provides a logic 1 signal.

26. (New) The memory circuit of claim 9, wherein a voltage of the second bit line is brought to an intermediate voltage when the first column of memory cells is selected.

27. (New) The memory circuit of claim 26, wherein the intermediate voltage is approximately  $V_{dd}/2$ .

28. (New) The memory circuit of claim 26, wherein the second bit line is coupled to an amplifier that reduces the voltage of the second bit line to the intermediate voltage when the first column of memory cells is selected.

29. (New) The memory circuit of claim 9, wherein the memory circuit is a read-only-memory circuit.